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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,113	06/12/2002	Chien-Hung Liu	MXIP0042USA	9179

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
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EXAMINER	
BARRECA, NICOLE M	

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 12/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/064,113	LIU ET AL.
	Examiner	Art Unit
	Nicole M. Barreca	1756

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-20 are pending in this application.

Specification

2. The abstract of the disclosure is objected to because it is longer than 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Lai (US 6,432,778).

The applied reference has a common inventors and assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Lai discloses a method for forming a system on chip (SOC) with nitride read only memory (NROM) and mask read only memory (cl.20) (col.1, 7-11). Semiconductor wafer 101 comprises a P type silicon substrate 102 including a periphery area 103 and memory area 104. The read only memory (ROM) area comprises NROM 105 and ROM 106. The ROM area further comprises at least one low voltage threshold device area and at least one high voltage threshold device area. N and P type ion implantations are performed in the periphery area 103 (cl.6,7). A plurality of isolators such as a field oxide layer is formed to isolate the periphery area, the NROM area and define the active area. ONO dielectric layer 118 (bottom oxide 112, silicon nitride 114, top oxide 116) is formed, followed by first photoresist layer 121. The bottom oxide is formed at a thickness of 50-150 angstroms using LPCVD at 750-1000 °C (cl.3). The silicon nitride layer is formed at a thickness of 100-300 angstroms using LPCVD (cl.4). The top oxide layer is formed a thickness of 50-200 angstroms using wet oxidation (cl.5). The first photoresist is patterned to define bit lines and a (first) etching is performed to remove uncovered portions of layers 116,114,112. A (first) ion implantation is performed to form a plurality of N+ doping areas for use as buried bit lines 122. A first and a second angled ion implantation are performed (cl.8-11). First photoresist 121 is removed and an etching process is performed to remove the ONO layer in the periphery area (cl.12) (col.4, 7-col.5, 67). A thermal oxidation process is performed to form a buried drain oxide layer atop each bit line 122 (col.5, 64-66). A polysilicon layer or a polysilicon layer comprising a polysilicide layer on top (cl.18) and a second photoresist layer are formed. The second photoresist is patterned to define a plurality of word lines in the memory

area and a plurality of gates in the periphery area. The polysilicon layer is then etched using the second photoresist as a mask in order to simultaneously form the word lines 134 in the memory area and gate 138 of the periphery transistor in the periphery area (cl.13). The second photoresist is removed. At least one NROM 142 is formed in the NROM area 105. A low voltage Vth device 144 is formed in the low voltage Vth area 107 and a high voltage Vth device 146 is formed in the high voltage Vth area 108 in the ROM area 106 (col.6, 19-40). A photoresist layer 152 is used to cover the low Vth area 107 in the ROM area and another threshold voltage adjustment ion implantation process is performed to implant P-type dopant into the high Vth area (ROM code implantation). The photoresist 152 covers the buried drain. The photoresist 152 is removed (cl.14-17) (col.6, 41-58). The high Vth and low Vth devices can represent 0&1 or 1&0 to achieve date storage (cl.19) (col.6, 59-64).

5. Claims 1-18, 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Lai (US 6,448,126).

The applied reference has a common inventors and assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Lai discloses a method for forming a system on chip (SOC) with nitride read only memory (NROM), such as mask ROM (cl.20) (col.1, 10-26). Semiconductor wafer 101 comprises a P type silicon substrate 102 including a periphery area 103 and memory area 104. N and P type ion implantations are performed in the periphery area 103 to adjust the threshold voltage (cl.6,7). A plurality of isolators such as a field oxide layer is formed to isolate the periphery area, the NROM area and define the active area. ONO dielectric layer 112 (bottom oxide 108, silicon nitride 109, top oxide 110) is formed, followed by first photoresist layer 115. The bottom oxide is formed at a thickness of 50-150 angstroms using LPCVD at 750-1000 °C (cl.3). The silicon nitride layer is formed at a thickness of 100-300 angstroms using LPCVD (cl.4). The top oxide layer is formed a thickness of 50-200 angstroms using wet oxidation (cl.5). The previously mentioned ion implantation process for adjusting the threshold voltage can be preformed at this point. The first photoresist is patterned to define bit lines and a (first) etching is performed to remove uncovered portions of layers 108,109,110. A (first) ion implantation is performed to form a plurality of N+ doping areas for use as buried bit lines 116. A first and a second angled ion implantation are performed (cl.8-11). First photoresist 115 is removed and a (second) etching process is performed to remove the ONO layer in the periphery area (cl.12) (col.4, 21-col.5, 67). A thermal oxidation process is performed to form a buried drain oxide layer 128 atop each bit line 116 (col.6, 6-18). A third photoresist and etching process is performed to form a N-well. A fourth photoresist and etching process is used to form the P-well (cl.14-16) (col.6,19-43). A polysilicon layer or a polysilicon layer comprising a polysilicide layer on top (cl.18) and a second photoresist

layer 144 are formed. The second photoresist is patterned to define a plurality of word lines in the memory area and a plurality of gates in the periphery area. The polysilicon layer is then etched using the second photoresist as a mask in order to simultaneously form the word lines 146 and gate 156 (cl.13). The second photoresist is removed. At least one NROM 142 is formed in the NROM area 105.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 of U.S. Patent No. 6432778. Although the conflicting claims are not identical, they are not patentably distinct from each other because the both claim the same method steps for forming ROM and NROM with a low and a high threshold voltage device areas. The conflicting claims are not identical because all of the process steps are not in the exact same order and some additional process steps are present in one set of claims and not the other.

However both sets of claims are written in open language without specifying a sequential order and therefore are not patently distinct from each other.

8. Claims 1-18, 20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-11 of U.S. Patent No. 64448126. Although the conflicting claims are not identical, they are not patentably distinct from each other because the both claim the same method steps for forming NROM. The conflicting claims are not identical because all of the process steps are not in the exact same order and some additional process steps are present in one set of claims and not the other. However both sets of claims are written in open language without specifying a sequential order and therefore are not patently distinct from each other.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nicole M. Barreca whose telephone number is 703-308-7968. The examiner can normally be reached on Monday-Thursday (8:00 am-6:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 703-308-2464. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9310.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Nicole Barreca

NICOLE BARRECA
PATENT EXAMINER

12/8/03